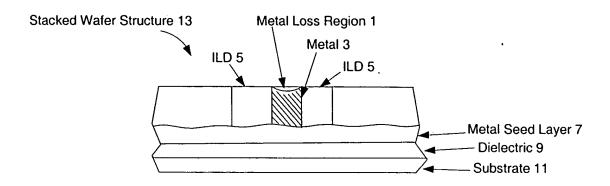
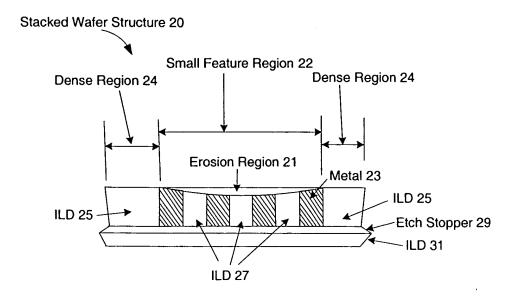
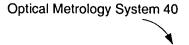
Sheet 1 of 10

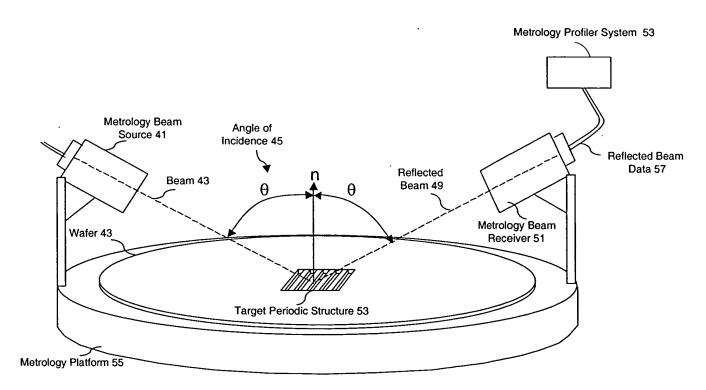


## **FIGURE 1A PRIOR ART**



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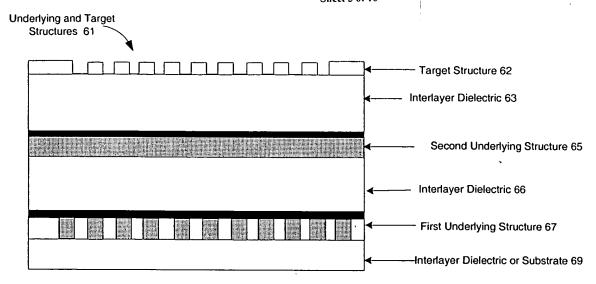


FIGURE 3A

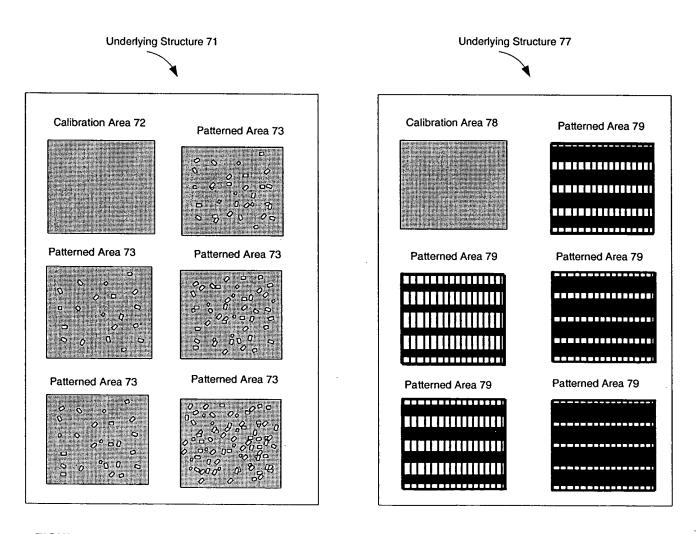
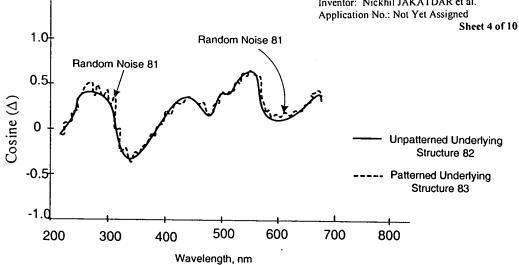


FIGURE 3B FIGURE 3C



**FIGURE 4A** 

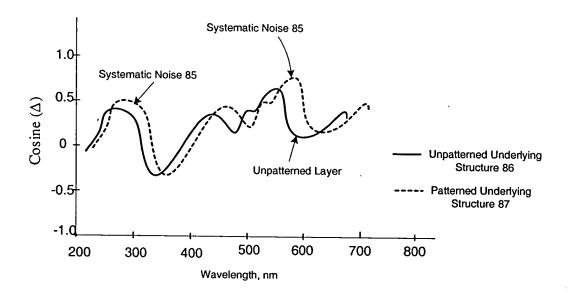


FIGURE 4B

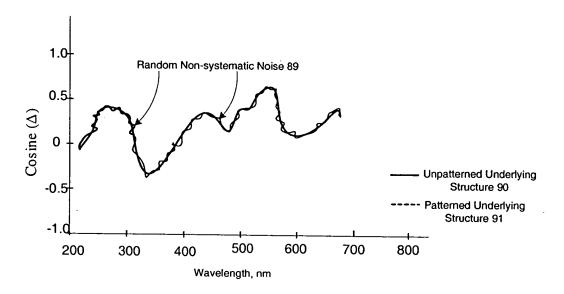


FIGURE 4C

Title: BALANCING PLANARIZATION OF LAYERS AND THE EFFECT OF et al. Inventor: Nickhil JAKATDAR et al. Application No.: Not Yet Assigned Sheet 5 of 10  $50~\mu m$ Underlying Structure 95  $20 \mu m Pad$ **Underlying Structure 97** -25 µm Pad **Underlying Structure 99** - 30 μm Pad

FIGURE 5

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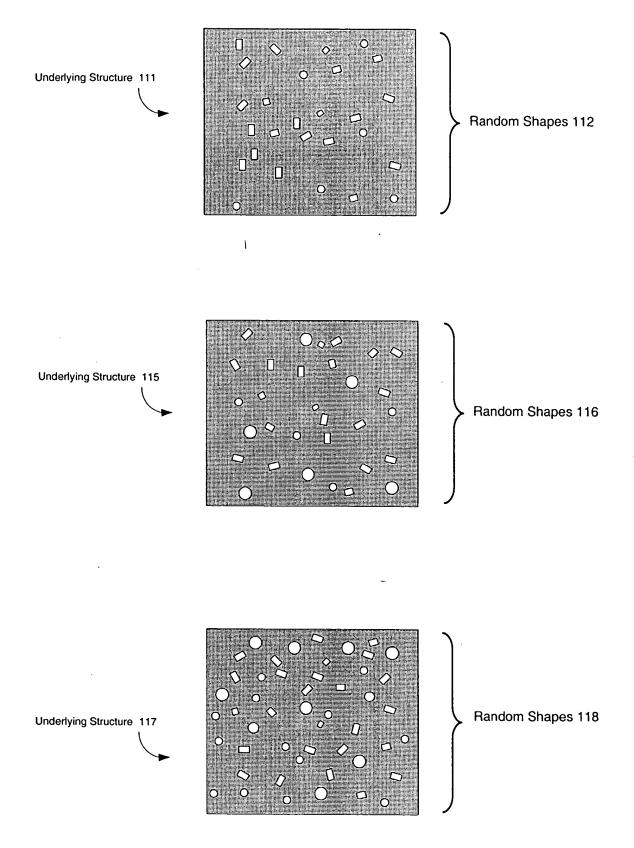
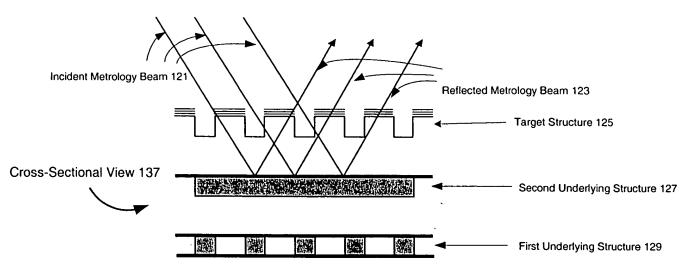
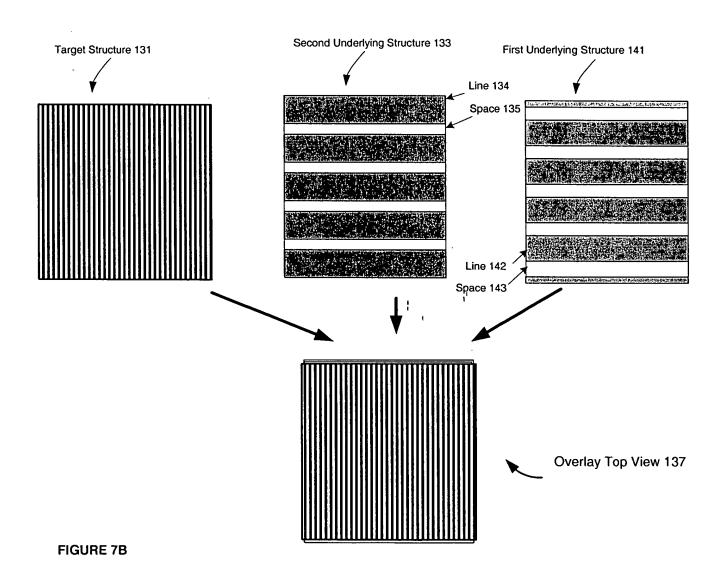


FIGURE 6

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## **FIGURE 7A**



Application No.: Not Yet Assigned Sheet 8 of 10 200 Set CMP and optical metrology signal design criteria. 210 Design the predetermined underlying structures in the wafer. 220 Fabricate the predetermined underlying structures and the subsequent layers of the wafer. 230 Measure CMP process characteristics. 250 Fabricate target structures in the target layer of the wafer. 260 Measure the reflected optical Alternative metrology signal from a calibration test area in the target layer of the 295 wafer. Calculate the reflected optical signal off target 270 structures. Measure the reflected electromagnetic signal from different target structures in the target layer of the wafer. 280 Identify the target structure design with the best fitting reflected optical metrology signal compared to the calibration signal. 290 No CMP and optical metrology design criteria met? Yes

Title: BALANCING PLANARIZATION OF LAYERS AND THE EFFECT OF et al. Inventor: Nickhil JAKATDAR et al.

FIGURE 8

Jacob Layer Profiler

300
Underlying Structure Designer

320
Wafer Fabricator

Wafer Fabricator

Designer

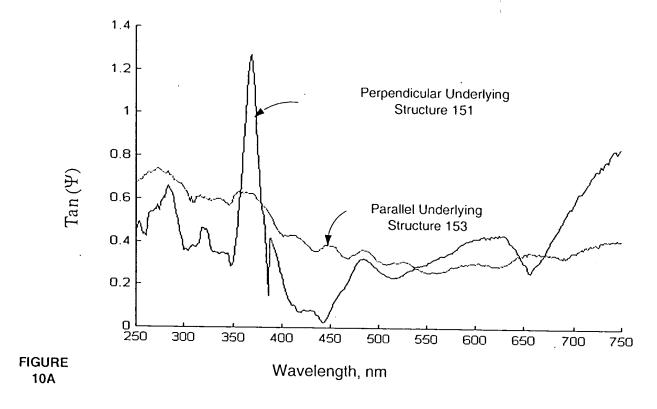
370

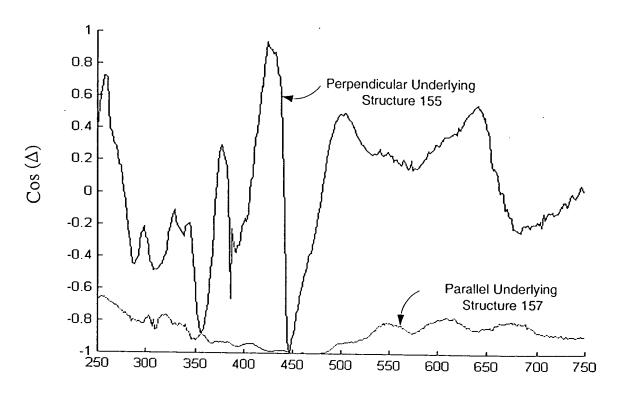
Reflected Metrology Signal Estimator 350

Design Selector

FIGURE 9

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Wavelength, nm

FIGURE 10B